**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-16. (Canceled)

17. (Currently Amended) An integrated circuit comprising at least a digital part comprising a plurality of transistors connected to one another so as to form a plurality of functional elements, the functional elements being grouped in subassemblies each comprising a first and a second electrical supply terminal and a clock input, the subassemblies being ~~connected in~~ powered in a series arrangement by their supply terminals ~~to the~~ from terminals of a voltage supply source,

wherein a same clock signal is applied to the clock input of all subassemblies, by a device for shifting the levels of the clock ~~signal, and~~signal.

~~wherein the subassemblies are formed in such a way that a same current flows through each of the subassemblies.~~

18. (Previously Presented) Integrated circuit according to claim 17, wherein the clock inputs of at least two adjacent subassemblies are connected by a device for shifting the clock signal levels.

19. (Previously Presented) Integrated circuit according to claim 18, wherein the clock input of an end subassembly is connected by an additional device for shifting the clock signal levels at the output of the clock circuit.

20. (Previously Presented) Integrated circuit according to claim 17, wherein the device for shifting the clock signal levels comprises at least one capacitor.

21. (Previously Presented) Integrated circuit according to claim 17, wherein the device for shifting the clock signal levels comprises at least one transistor.

22. (Previously Presented) Integrated circuit according to claim 17, wherein all the subassemblies are identical.

23. (Previously Presented) Integrated circuit according to claim 17, wherein each of the subassemblies comprises a voltage limiting circuit connected between the first and the second electrical supply terminals.

24. (Previously Presented) Integrated circuit according to claim 23, wherein the voltage limiting circuit comprises a diode.

25. (Previously Presented) Integrated circuit according to claim 23, wherein the voltage limiting circuit comprises a transistor.

26. (Previously Presented) Integrated circuit according to claim 17, wherein each subassembly comprises a decoupling capacitor connected between the first and the second electrical supply terminals of the subassembly.

27. (Previously Presented) Integrated circuit according to claim 17, wherein the integrated circuit comprises electrical insulation between the subassemblies.

28. (Previously Presented) Integrated circuit according to claim 27, wherein the electrical insulation between the different subassemblies comprises reverse biased diode junctions.

29. (Previously Presented) Integrated circuit according to claim 27, wherein the electrical insulation between the different subassemblies comprises dielectric zones.

30. (Previously Presented) Integrated circuit according to claim 17, wherein the integrated circuit comprises silicon blocks from a silicon-on-insulator substrate.

31. (Previously Presented) Integrated circuit according to claim 17, wherein the subassemblies are at different electrical potentials,

wherein a potential difference between two end subassemblies is greater than a potential difference between terminals of each subassembly.

32. (Previously Presented) Integrated circuit according to claim 17, wherein a voltage level of the clock signal applied to the clock input of each subsassembly is adapted to voltages present at the first and second electrical supply terminals of the corresponding subassembly.

33. (Previously Presented) Integrated circuit according to claim 17, wherein the same current flowing through the different subassemblies varies by less than 20%.

34. (Previously Presented) Integrated circuit according to claim 17, wherein the subassemblies are formed in such a way that, at all times in operation, the same current flows through each of the subassemblies.

35. (Currently Amended) A method of controlling current in an integrated circuit comprising:

applying a same clock signal to a clock input of all subassemblies via a device for shifting the levels of the clock signal, the subassemblies being in a structure in which an integrated circuit comprises at least a digital part comprising a plurality of transistors connected to one another so as to form a plurality of functional elements, the functional elements being grouped in subassemblies each comprising a first and a second electrical supply terminal and a clock input, the subassemblies being ~~connected in~~ powered in a series arrangement by their supply terminals ~~to the~~from terminals of a voltage supply ~~source,~~source.

~~wherein the subassemblies are formed in such a way that, at all times, the same current flows through each of the subassemblies.~~

36. (New) A power supply system for an integrated circuit comprising:

a power supply;

an integrated circuit, the integrated circuit further comprising:

at least a digital part comprising a plurality of transistors connected to one another so as to form a plurality of functional elements, the functional elements being

grouped in subassemblies each comprising a first and a second electrical supply terminal and a clock input, the subassemblies being powered in a series arrangement by connecting a second supply terminal of a subassembly to a first supply terminal of a next subassembly in the series arrangement, and connecting the first supply terminal of a first subassembly in the series arrangement and the second supply terminal of a last subassembly in the series arrangement across the power supply; and

a clock circuit providing an identical clock signal to the clock input of each one of the subassemblies via a device for shifting the levels of the clock signal.